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(54) **A constant current circuit and an oscillating circuit controlled by the same**
Konstantstromschaltung und ein Schwingkreis gesteuert durch dieselbe
Circuit de courant constant et un circuit oscillant commandé par ledit circuit

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(56) References cited:
EP-A- 0 165 748 **EP-A- 0 263 572**

- **IBM TECHNICAL DISCLOSURE BULLETIN. vol. 19, no. 4, September 1976, NEW YORK US pages 1375 - 1376 J. D. LEPAGE ET AL. 'Voltage-To-Current Converter'**
- **ELECTRONIC LETTERS; vol.26, no.10; May 1990; pgs.619-620.**

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Description

The present invention relates to a constant current circuit, which can be used for example to control an oscillating circuit for providing a variable-frequency clock generator in a battery-powered computer.

Various methods for saving electric power are implemented in computers powered by batteries. For example, the operating voltage is reduced in operation modes not requiring high speed, e.g. mode selection prior to arithmetic processing, together with lowering the clock signal frequency. The lower operating voltage and lower clock signal frequency both help to reduce power consumption.

In conventional battery-powered computers, one of the following techniques is used for changing the clock signal frequency. The first is to provide multiple oscillators for generating clock signals of different frequencies, and to select a suitable one of the oscillators when performing, for example, a high-speed operation such as arithmetic processing or a low-speed operation such as mode selection. The second is to provide a single oscillator of a relatively high frequency, and obtain a desired low frequency by demultiplying the high frequency. However, both these techniques involve drawbacks of requiring extra hardware such as oscillators and selecting circuits, and of increase in the cost of the computers. Another drawback of the conventional techniques is that the clock frequency cannot be continuously varied.

Electronics Letters, vol. 26, no. 10, 1st May 1990, pages 619 - 621 discloses a bipolar linear transconductor having the features of the preamble of accompanying claim 1. The transconductor receives an input voltage independently of a power voltage.

IBM Technical Disclosure Bulletin, vol. 19, no. 4, September 1976, pages 1375 - 1376, discloses a voltage-to-current converter in which an output current is linearly related to an input voltage difference. The input voltage is for example a difference between a video output voltage from an optical scanner and a black-peak reference voltage.

According to the present invention, there is provided a constant current circuit having a source for supplying a power voltage, constant current supplying means including at least one constant current supplying source, first and second transistors connected between the power voltage supplying source and the constant current supplying means, each of the transistors having a control electrode, and a resistance means including at least one resistor, connected between respective nodes of the first and second transistors and connected to the constant current supplying means characterised in that the control electrode of the first transistor is provided with a reference voltage and the constant current circuit further comprises a voltage divider providing a divided voltage of the power voltage for the control electrode of the second transistor, whereby the current flowing in the second transistor is controlled according to the magnitude of said power voltage, and the rate of change of the current with respect to change of the power voltage depends on the resistance of the resistance means, said resistance being chosen such that the second transistor outputs a current which linearly changes with the power voltage.

The present invention may be applied to control of an oscillating circuit capable of generating clock signals of higher frequency for operations such as arithmetic processing and of lower frequency for operations such as mode selection, with a simple circuit configuration and at low cost, and/or to an oscillating circuit which generates higher or lower frequency clock signals in response to a change in the power source voltage, for example having an oscillation frequency which can be continuously changed by changing the power source voltage.

Reference will now be made, by way of example, to the accompanying drawings in which:-

Fig. 1 is a diagram showing the fundamental configuration of a constant current circuit of the present invention;
Fig. 2 is a diagram showing the fundamental configuration of an oscillating circuit which can be controlled by means of the present invention;
Fig. 3 is a graph showing the relationship between power voltage V_{cc} and current I_2 in the constant current circuit of Fig. 1;
Fig. 4 is a graph for explaining the change of the slope of the V_{cc}-I_2 characteristic curve of Fig. 3 with the change of R_4;
Fig. 5 shows waveforms of the signal output from the oscillating circuit of Fig. 2, corresponding to different power voltages V_{cc} in the constant current circuit of Fig. 1;
Fig. 6 is a graph showing the relationship between power voltage V_{cc} in the circuit of Fig. 1 and oscillation frequency f in Fig. 2;
Fig. 7 is a graph showing the change of the slope of the V_{cc}-f curve of Fig. 6 with the change of R_4;
Fig. 8 is a graph for explaining an extended change of I_2 in the V_{cc}-I_2 characteristic of Fig. 3;
Fig. 9 is a graph for explaining an extended change of f in the V_{cc}-f characteristic of Fig. 6;
Fig. 10 is a diagram showing the fundamental configuration of another constant current circuit of the present invention;
Fig. 11 is a diagram showing a first embodiment of the present invention;
Fig. 12 is a graph for explaining the shift of I_4 in the circuit of Fig. 11;
Fig. 13 is a graph for explaining the shift of frequency f in the circuit of Fig. 11;
Fig. 14 shows waveforms of the signal output from the circuit of Fig. 11, corresponding to different values of V_{cc};
Fig. 15 is a diagram showing a second embodiment of the present invention;
Fig. 16 shows waveforms of the signal output from

the circuit of Fig. 15, corresponding to different values of V_{cc};

Fig. 17 is a diagram showing a third embodiment of the present invention;

Fig. 18 is a graph showing the V_{cc}-I_4 characteristic of the circuit of Fig. 17;

Fig. 19 is a graph showing the V_{cc}-f characteristic of the circuit of Fig. 17; and

Fig. 20 shows waveforms of the signal output from the circuit of Fig. 17 for different values of V_{cc}.

A constant current circuit of the present invention is shown in Fig. 1, which comprises a reference voltage source block 1, a differential amplifier block 3 including a constant current supplying source block 2 and a resistor R_4, and a voltage dividing block 4 for dividing a power source voltage V_{cc}.

Differential amplifier block 3 comprises transistors Q_3 and Q_5, e.g. bipolar transistors each having a collector connected to the power source voltage V_{cc} and an emitter connected to one of the constant current supplying sources I_A and I_B. The base (control electrode) of the transistor Q_3 is supplied with a reference voltage V_1 from the reference voltage source block 1 and the base of transistor Q_5 is supplied with a divided voltage V_2 of power source voltage V_{cc} from the node of resistors R_2 and R_3 constituting the voltage dividing block 4. The resistor R_4 is connected between the emitters of the transistors Q_3 and Q_5. Hence, a current I_2 dependent on the difference between the voltages V_1 and V_2 flows through the collector of transistor Q_5. The transistor Q_4 provided between the power voltage source V_{cc} and the collector of transistor Q_5 constitutes a current mirror in co-operation with the transistor Q_6. The transistors Q_4 and Q_6 are bipolar transistors, for example, each having an emitter connected to the power voltage source V_{cc} and their bases connected to each other. The base of the transistor Q_4 is also connected to its collector.

Characteristics and operation of the constant current circuit of in Fig. 1 are described later.

To explain an application of the constant current circuit of the invention, the fundamental configuration of an oscillating circuit is as shown in Figure 2, which comprises a current integration block 6 and a charge-discharge control block 7. The current integration block 6 includes aforementioned transistor Q_6 constituting a current mirror 5, and a capacitor C_0 connected between the collector of the transistor Q_6 and ground potential source. The capacitor C_0 is charged with a current I_4 which is substantially equal to the current I_2 flowing through the transistor Q_4, and the potential V_0 at a terminal of the capacitor C_0 increases with the charging. The charge-discharge control block 7 includes a voltage detection circuit D_1 and a switch means SW. The voltage detection circuit D_1 detects the voltage V_0 of the capacitor C_0 and instructs the switch means SW to close on detecting V_0 higher than a first predetermined voltage (V_{S1}) and to open on detecting V_0 lower than a second predetermined voltage (V_{S2}). Hence, the capacitor C_0 is subject to be charged or discharged along with the ON-OFF operation of the switch means SW, and V_0 changes as a triangular wave of a constant frequency. The frequency can be varied by changing the power source voltage V_{cc} as described later.

Referring again to Fig. 1 together with Fig. 3, the resistors R_2 and R_3 are selected so that V_2 is equal to V_1 when the power source voltage V_{cc} is V_4, hence, $I_2 = I_B$ and the current I_3 flowing through the resistor R_4 is zero. Under this condition, if the power source voltage V_{cc} is increased higher than V_3, V_2 becomes larger than V_1, hence, the current I_2 increases while the current I_1 decreases. Accordingly, the current I_3 flows through the resistor R_4 from the transistor Q_5 to the constant current supplying source I_A. At a higher power source voltage V_5, the current I_1 flowing through the transistor Q_3 becomes almost zero, hence, $I_2 = I_A + I_B$. If the power source voltage V_{cc} is decreased lower than V_4, V_2 becomes smaller than V_1, hence, the current I_1 increases while the current I_2 decreases. Accordingly, the current I_3 flows through the resistor R_4 from the transistor Q_3 to the constant current supplying source I_B. At a lower power source voltage V_3, the current I_2 flowing through the transistor Q_5 becomes almost zero, hence, $I_2 = 0$. As described above, the direction of I_3 flowing through R_4 is reversed at a V_{cc} where $V_{cc} = V_4$, and I_2 can be changed continuously with V_{cc} so as to be larger than I_B in a range where $V_{cc}>V_4$ and to be smaller than I_B in a range where $V_{cc}<V_4$. If V_{cc} is in the range of $V_3(V_{cc}<V_4$, I_2 is represented by $I_2 = I_B - I_3$, hence, $I_2 \fallingdotseq I_B -(V_1-V_2)/R_4$, while, if V_{cc} is in the range of $V_4<V_{cc}<V_5$, I_2 is represented by $I_2 = I_B + I_3$, hence, $I_2 \fallingdotseq I_B +(V_2-V_1)/R_4$. Accordingly, the larger the resistance of the resistor R_4, the larger the current I_2 in the range of $V_3(V_{cc}<V_4$, while, the larger the resistance of the resistor R_4, the smaller the current I_2 in the range of $V_4<V_{cc}<V_5$. Thus, the slope of the V_{cc}-I_2 characteristic curve shown in Figure 3 becomes gentle with respect to the increase in R_4. Such change in the V_{cc}-I_2 characteristic curve by the resistance of the resistor R_4 is shown in Figure 4. Accordingly, I_2 can continuously be changed with the change of V_{cc}, if the resistor R_4 is selected to have an enough large resistance. This feature enables the oscillating circuit of Figure 2 to be a variable frequency oscillator.

The operation of the oscillating circuit of Figure 2 with the change of the power source voltage V_{cc} is described in the following.

The current I_4 to charge the capacitor C_0 of the oscillating circuit is equal to I_2 flowing through the transistor Q_4 in the constant current circuit of Figure 1, due to the function of the current mirror comprising the transistors Q_4 and Q_6. Hence, the rate of charging the capacitor C_0 depends on the current I_2 which can be controlled by changing the power source voltage V_{cc}. On the other hand, the rate of discharging the capacitor C_0 is constant regardless of the change of V_{cc}. Therefore, the frequency of oscillating circuit of Figure 2 changes according to

the change of the power source voltage V_{cc}. Figure 5 shows exemplary waveforms of the signal output from the oscillating circuit of Figure 2, corresponding to aforementioned specific V_{cc}s of V_3, V_4 and V_5, and Figure 6 shows the change in the frequency of the output signal with respect to the change of V_{cc}. In Figure 5, V_{S1} and V_{S2} represent the maximum and minimum of the voltages V_0 at an end of the capacitor C_0, respectively, which are detected by the voltage detection circuit D_1 as described above with reference to Figure 2. On other words, V_{S1} is a voltage V_0 where the discharging of the capacitor C_0 initiates, and, V_{S2} is a voltage V_0 where the charging of the capacitor C_0 initiates. As shown in Figure 5, the rise time of the output signal decreases as V_{cc} increases, while the fall time of the signal is constant because it only depends on the resistance inherent in the switching means SW shown in Figure 2. At a power source voltage where $V_{cc} = V_3$, the frequency of the output signal is zero as shown in Figures 5 and 6, because the current I_4 becomes zero and the capacitor C_0 is not charged.

As mentioned before with reference to Figure 4, the slope of V_{cc}-I_2 characteristic curve becomes gentle by increasing the resistance of the resistor R_4. Accordingly, the slope of V_{cc}-f characteristic curve shown in Figure 6 becomes gentle with the increase of R_4 as shown in Figure 7. Thus, it is possible to attain fine tuning of the oscillation frequency f by changing the power source voltage V_{cc}, and the circuit of Figure 2 can be a variable frequency oscillator. It is obvious that if R_4 is decreased to zero, the slope of V_{cc}-I_2 characteristic curve of Figure 4, and hence, the slope of V_{cc}-f characteristic curve of Figure 7 become so steep that the circuit of Figure 2 could not be used as a variable frequency oscillator.

Referring back to Figure 1, if the constant current supplying sources I_A and I_B are replaced by corresponding ones having larger current capacities I_A' and I_B', respectively, the change of I_2 in the V_{cc}-I_2 characteristic curve of Figure 3 is extended as shown in Figure 8, hence, the change of f in the V_{cc}-f characteristic curve of Figure 6 is extended as shown in Figure 9. In Figures 8 and 9, respective dotted lines represent original V_{cc}-I_2 characteristic curve corresponding to that in Figure 3 and V_{cc}-f characteristic curve corresponding to that in Figure 6, and f_4' and f_5' respectively indicate the frequencies f_4 and f_5 changed according to the increase in I_A and I_B.

Figure 10 is a diagram showing the fundamental configurations of another constant current circuit of the present invention. The circuit, comprising a reference voltage source 1, a differential amplifier block 3 and a voltage dividing block 4 for dividing power source voltage V_{cc}, is almost the same as the circuit of Figure 1, except for that the Figure 10 circuit includes only one constant current supplying source I_D connected to a point on the resistor R_4, the point dividing R_4 into two parts R_{41} and R_{42}. If R_4 is equally divided, i.e. $R_{41} = R_{42}$, the constant current circuit of Figure 10 has the same characteristics as that of the circuit of Figure 1. The feature of R_4 to change the slope of the V_{cc}-I_2 characteristics is also provided. When R_4 is not equally divided, i.e. $R_{41} \neq R_{42}$, the V_{cc}-I_2 characteristic curve regarding the circuit shifts along the V_{cc} axis, wherein the direction and amount of the shift depends on the ratio R_{41}/R_{42}.

The first embodiment of the constant current circuit of the present invention is shown in Figure 11. The constant current circuit has a configuration based on that of Figure 1 and is applied to control of an oscillating circuit with a configuration based on Figure 2. This embodiment circuit is provided with an additional constant current supplying block 8 including a current mirror comprising transistors Q_7 and Q_8, both bipolar transistors, for example, and a constant current supplying source I_C connected to the collector of the transistor Q_8. The current I_4 for charging the capacitor C_0 is increased by the current I_C such as represented by $I_4 \fallingdotseq I_2 + I_C$. Thus, the current I_4 shifts larger by I_C as shown in Figure 12, wherein the dotted line represents the original V_{cc}-I_4 characteristic curve corresponding to that in Figure 3. As a result of the shift, I_4 is not zero but I_C at $V_{cc} = V_3$, different from V_{cc}-I_2 characteristic curve corresponding to that of the circuit shown in Figure 1, in which I_2 is equal to I_4, hence, I_4 is zero at $V_{cc} = V_3$. Accordingly, the range of the oscillation frequency of the Figure 11 circuit shifts higher by Δf as shown in Figure 13, wherein the frequency f is not zero but f_3 at $V_{cc} = V_3$. In Figure 13, the dotted line represents the original V_{cc}-f characteristic curve corresponding to Figure 6. Waveforms of the signal output from the circuit of Figure 11 are shown in Figure 14, corresponding to the specific V_{cc}s of V_3, V_4 and V_5.

The second embodiment of the present invention is shown in Figure 15. The constant current circuit again has a configuration based on that of Figure 1, and is used to control an oscillating circuit of the Figure 2 type

The oscillator is provided with an additional constant current supplying source I_0 connected in series to the switching means SW in the charge-discharge control block 7. With the addition of the constant current supplying source I_0, the current flowing through the switching means SW during discharging the capacitor C_0 is increased or decreased.

If the current I_0 is selected as $I_0 = nI_4$, the ratio of the time for discharging to the time for charging of the capacitor C_0 is represented by 1/(n-1), wherein n represents a positive number larger than 1. Thus, the rise time to fall time ratio of the signal output from the circuit of Figure 15 can be controlled, depending on the current capacity of the constant current supplying source I_0. Waveforms of the signal output from the circuit of Figure 15 in which the constant current supplying source I_0 has a current capacity of $I_0 = 2\ I_4$ are shown in Figure 16, corresponding to the specific V_{cc}s of V_3, V_4 and V_5. As seen in Figure 16, the duty factor of each waveform is 50%.

The third embodiment of the present invention is shown in Figure 17, wherein the constant current circuit again has a configuration based on Figure 1 and is

shown with an oscillating circuit of the Figure 2 type. Constant current supplying sources I_C and I_0 are provided, as explained above with reference to Figures 11 and 15. In the circuit of Figure 17, the transistors Q_1 and Q_2, both bipolar transistors, for example, and a resistor R_1 constitute a source of reference voltage V_1. The base-emitter junction voltage of the transistors Q_1 and Q_2 which are connected to each other in series and supplied with a bias current is used as a constant voltage source. In Figure 17, a transistor Q_3 is used as a switching means and a Schmitt circuit D_2 is used as a voltage detection circuit, respectively corresponding to those denoted by reference symbols SW and D_1 in Figure 11 and 15. The Schmitt circuit D_2 converts triangular pulse signals into rectangular pulse signals thanks to the waveform shaping function thereof based on the inherent hysteresis characteristics between the input and output. The V_{cc}-I_4 characteristics and the V_{cc}-f characteristics of the circuit of Figure 17 are as shown in Figures 18 and 19, respectively.

In the circuit of Figure 17, the Schmitt circuit D_2 has two threshold values of a high level S_H and a low level S_L, and jumps the output F_{OUT} thereof to high level V_H, if V_O increases up to the high level threshold S_H. Hence, the transistor Q_9 turns on and the capacitor C_0 is discharged. Accordingly, the voltage V_0 decreases but the output remains at high level V_H. When the voltage V_0 reaches the low level threshold S_L, the Schmitt circuit D_2 jumps the output F_{OUT} to low level V_L. As a result, the transistor Q_3 turns off and the capacitor C_0 is stopped from discharging and begins charging by the current I_4. Hence, the voltage V_0 increases but the output remains at low level V_L until the voltage V_0 reaches the high level threshold S_H. Waveforms of the signal output from the circuit of Figure 17 are shown in Figure 20, corresponding to the specific power source voltages V_{cc} of V_3, V_4 and V_5. The waveforms are obtained when the constant current supplying source I_0 having a current capacity of $I_0 = 2\,I_4$ is used, and the rectangular pulses have a duty factor of 50%.

Any of the above embodiment circuits can be incorporated in a monolithic integrated circuit, therefore, they are suitably applied to computers like notebook-sized personal computers powered by batteries, hence, resulting in power savings of the computers by lowering the clock signal frequency and the power voltage during operations such as mode selection. The feature of variable frequency clock signals with the use of a single oscillating circuit also results in the reduction of hardware and production cost, while improving the reliability of the computers.

In the above description, examples have been given of circuits employing bipolar transistors. However, the present invention is also applicable to circuits employing other types of transistor such as FETs. In addition, the terms "resistor", "capacitor" and so forth refer to any device or circuit element (or combination of elements) having the desired property of resistance, capacitance, etc.

To summarise, the present invention concerns a constant current circuit whose output current I_2 can be varied with change of a power source voltage V_{cc}, which can be used to control an oscillating circuit whose oscillation frequency can be varied with change of the constant current circuit output current I_2, suitable for use in portable computers. In one form, the constant current circuit comprises bipolar transistors coupled to form a differential amplifier wherein one of the transistors is supplied with a reference voltage and the other is supplied with a divided voltage of the power source voltage V_{cc}, and a resistor connecting the emitters of the transistors is provided for controlling the slope of the V_{cc}-I_2 characteristic curve of the constant current circuit.

Claims

1. A constant current circuit having a source for supplying a power voltage (V_{cc}), constant current supplying means (I_A, I_B; I_D) including at least one constant current supplying source, first and second transistors (Q_3, Q_5) connected between the power voltage supplying source and the constant current supplying means, each of the transistors having a control electrode, and a resistance means (R_4) including at least one resistor, connected between respective nodes of the first and second transistors and connected to the constant current supplying means; characterised in that the control electrode of the first transistor (Q_3) is provided with a reference voltage (V_1) and the constant current circuit further comprises a voltage divider (R_2, R_3) providing a divided voltage of the power voltage (V_{cc}) for the control electrode of the second transistor;

   whereby the current flowing in the second transistor (Q_5) is controlled according to the magnitude of said power voltage, and the rate of change of the current with respect to change of the power voltage depends on the resistance of the resistance means (R_4), said resistance being chosen such that the second transistor (Q_5) outputs a current which linearly changes with the power voltage.

2. A constant current circuit as set forth in claim 1, wherein the constant current supplying means comprises two constant current supplying sources (I_A, I_B) each connected to a respective one of said nodes of the first and second transistors (Q_3, Q_5), and the resistance means comprises a single resistor (R_4) connected between said nodes of the first and second transistors and between the two constant current supplying sources.

3. A constant current circuit as set forth in claim 1, wherein the constant current supplying means comprises a single constant current supplying source (I_D), and wherein the resistance means (R_4) com-

prises first and second resistors (R_{41}, R_{42}) of equal resistance connected in series between said nodes of the first and second transistors (Q_3, Q_5), the single constant current supplying source (I_D) being connected to a node common to both the first and second transistors (R_{41}, R_{42}).

Patentansprüche

1. Eine Konstantstromschaltung mit einer Quelle zum Zuführen einer Energiespannung (V_{cc}), einem Konstantstromzuführmittel (I_A, I_B; I_D), das wenigstens eine Konstantstromzuführquelle enthält, ersten und zweiten Transistoren (Q_3, Q_5), die zwischen der Energiespannungszuführquelle und dem Konstantstromzuführmittel verbunden sind, von welchen Transistoren jeder eine Steuerelektrode hat, und einem Widerstandsmittel (R_4), das wenigstens einen Widerstand enthält und zwischen jeweiligen Knoten der ersten und zweiten Transistoren verbunden ist und mit dem Konstantstromzuführmittel verbunden ist; dadurch gekennzeichnet, daß die Steuerelektrode des ersten Transistors (Q_3) mit einer Referenzspannung (V_1) versehen ist und die Konstantstromschaltung ferner einen Spannungsteiler (R_2, R_3) umfaßt, der eine geteilte Spannung der Energiespannung (V_{cc}) für die Steuerelektrode des zweiten Transistors vorsieht;

   wodurch der Strom, der in dem zweiten Transistor (Q_5) fließt, gemäß der Größe der genannten Energiespannung gesteuert wird und die Veränderungsrate des Stromes bezüglich der Veränderung der Energiespannung von dem Widerstand des Widerstandsmittels (R_4) abhängt, welcher Widerstand so gewählt ist, daß der zweite Transistor (Q_5) einen Strom ausgibt, der sich mit der Energiespannung linear verändert.

2. Eine Konstantstromschaltung nach Anspruch 1, bei der das Konstantstromzuführmittel zwei Konstantstromzuführquellen (I_A, I_B) umfaßt, die jeweils mit einem entsprechenden der genannten Knoten der ersten und zweiten Transistoren (Q_3, Q_5) verbunden sind, und das Widerstandsmittel einen einzelnen Widerstand (R_4) umfaßt, der zwischen den genannten Knoten der ersten und zweiten Transistoren und zwischen den zwei Konstantstromzuführquellen verbunden ist.

3. Eine Konstantstromschaltung nach Anspruch 1, bei der das Konstantstromzuführmittel eine einzelne Konstantstromzuführquelle (I_D) umfaßt, und bei der das Widerstandsmittel (R_4) erste und zweite Widerstände (R_{41}, R_{42}) mit gleichem Widerstandswert umfaßt, die zwischen den genannten Knoten der ersten und zweiten Transistoren (Q_3, Q_5) seriell verbunden sind, welche einzelne Konstantstromzuführquelle (I_D) mit einem Knoten verbunden ist, der beiden Widerständen, sowohl dem ersten als auch dem zweiten, (R_{41}, R_{42}) gemeinsam ist.

Revendications

1. Circuit à courant constant ayant une source pour fournir une tension d'alimentation (Vcc), des moyens fournissant un courant constant (I_A, I_B; I_D) comprenant au moins une source fournissant un courant constant, des premier et deuxième transistors (Q3, Q5) montés entre la source fournissant une tension d'alimentation et les moyens fournissant un courant constant, chacun des transistors ayant une électrode de commande, et des moyens de résistance (R4), comprenant au moins une résistance, montés entre des noeuds respectifs des premier et deuxième transistors et connectés aux moyens fournissant un courant constant, caractérisé en ce que l'électrode de commande du premier transistor (Q3) reçoit une tension de référence (V1) et le circuti à courant constant comprend en outre un diviseur de tension (R2, R3) fournissant une tension divisée de la tension d'alimentation (Vcc) pour l'électrode de commande du deuxième transistor,

   ce par quoi le courant circulant dans le deuxième transistor (Q5) est commandé selon l'amplitude de ladite tension d'alimentation, et la vitesse de variation du courant par rapport à la variation de la tension d'alimentation dépend de la résistance des moyens de résistance (R4), ladite résistance étant choisie de telle manière que le deuxième transistor (Q5) fournisse un courant qui varie linéairement avec la tension d'alimentation.

2. Circuit à courant constant selon la revendication 1, dans lequel les moyens fournissant un courant constant comprennent deux sources fournissant un courant constant (I_A, I_B), chacune connectée à un noeud respectif desdits noeuds des premier et deuxième transistors (Q3, Q5), et les moyens de résistance comprennent une seule résistance (R4) montée entre lesdits noeuds des premier et deuxième transistors et entre les deux sources fournissant un courant constant.

3. Circuit à courant constant selon la revendication 1, dans leque les moyens fournissant un courant constant comprennent une seule source fournissant un courant constant (I_D), et dans lequel les moyens de résistance (R4) comprennent des première et deuxième résistances (R41, R42) d'égale résistance montées en série entre lesdits noeuds des premier et deuxième transistors (Q3, Q5), la source unique fournissant un courant constant (I_D) étant connectée à un noeud commun aux première et deuxième résistances (R41, R42).

FIG. 1

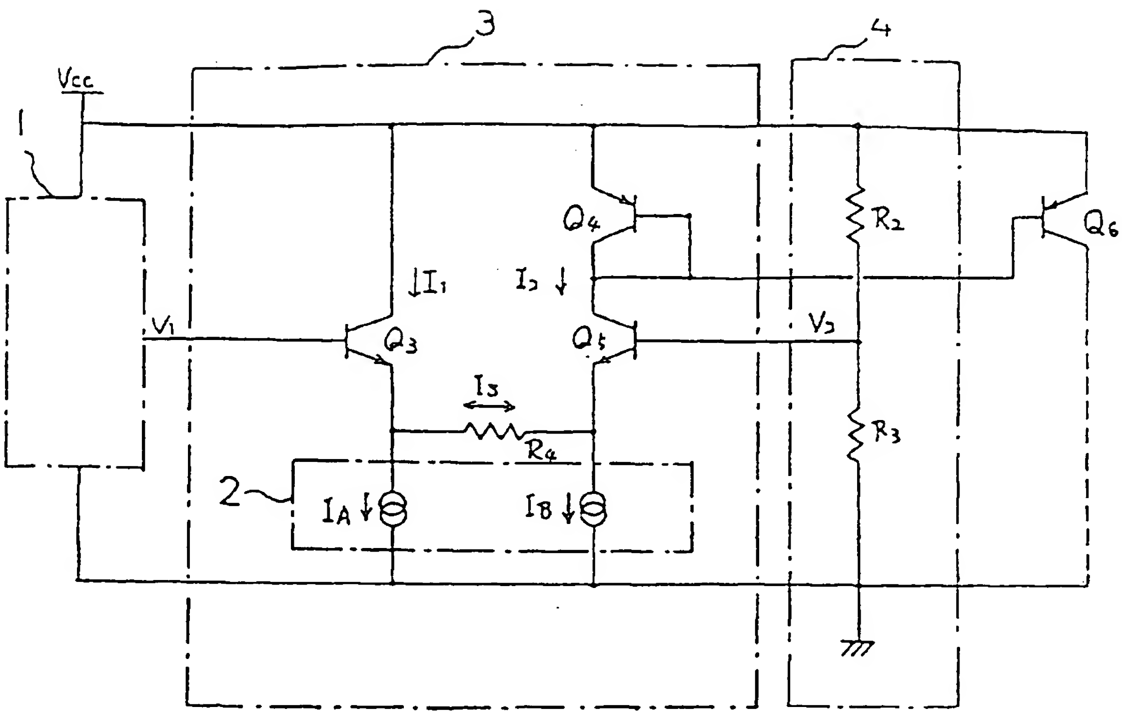

FIG. 2

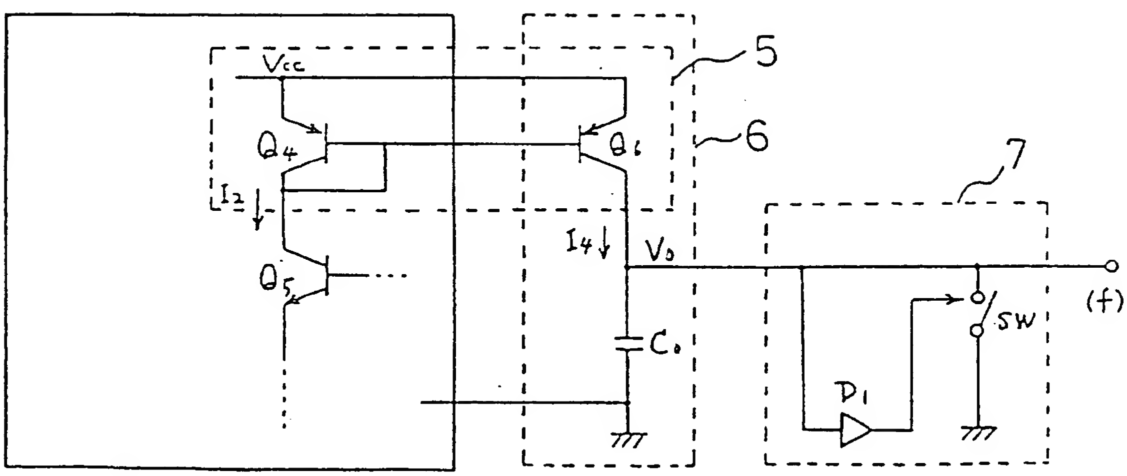

FIG. 3

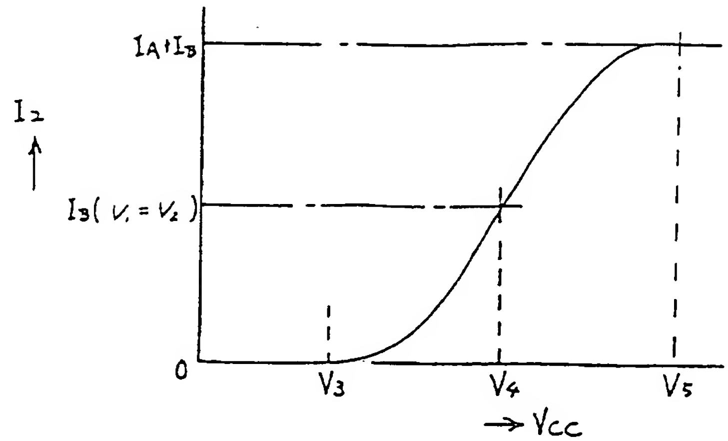
I_A+I_B
I_2
$I_B(V_1=V_2)$
0
V_3
V_4
V_5
→ Vcc

FIG. 4

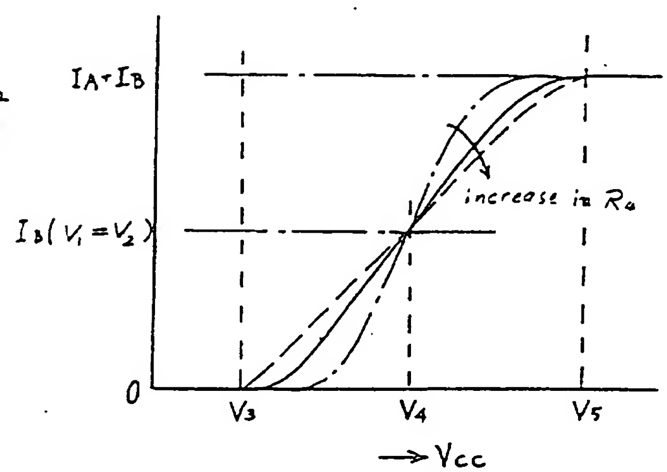
I_2
I_A+I_B
increase in R_4
$I_B(V_1=V_2)$
0
V_3
V_4
V_5
→ Vcc

FIG. 5

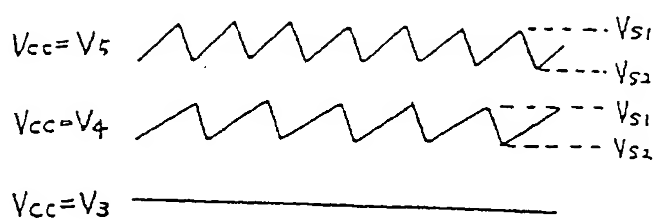

FIG. 6

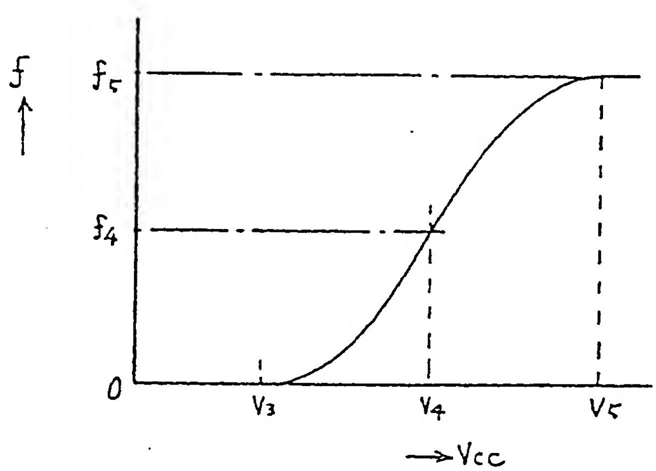

FIG. 7

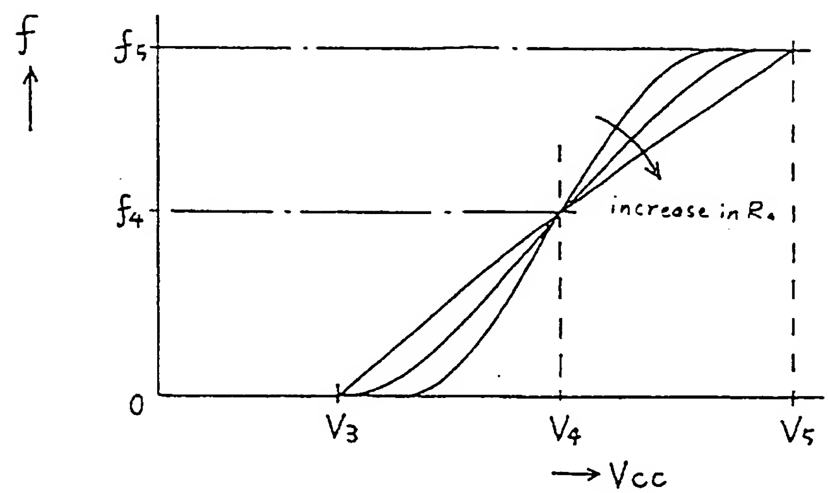

FIG. 8

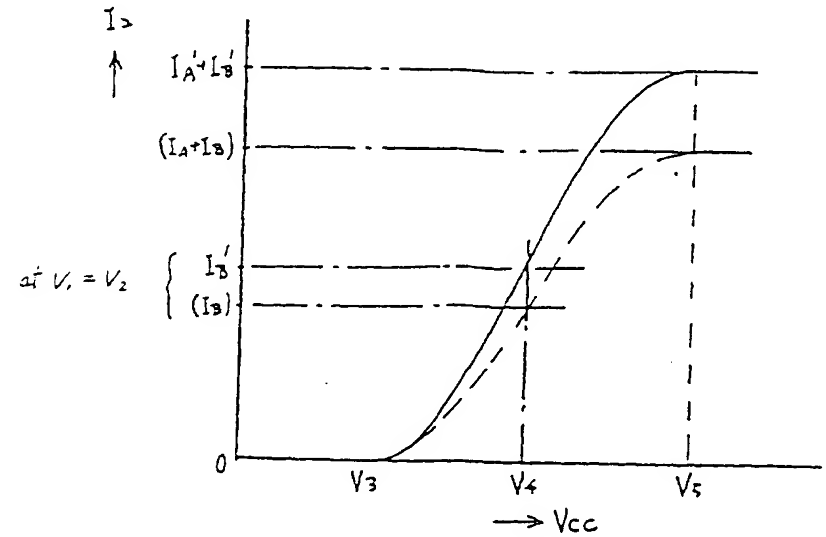
I_2
$I_A' + I_B'$
$(I_A + I_B)$
at $V_1 = V_2$
I_B'
(I_B)
0
V_3
V_4
V_5
→ Vcc

FIG. 9

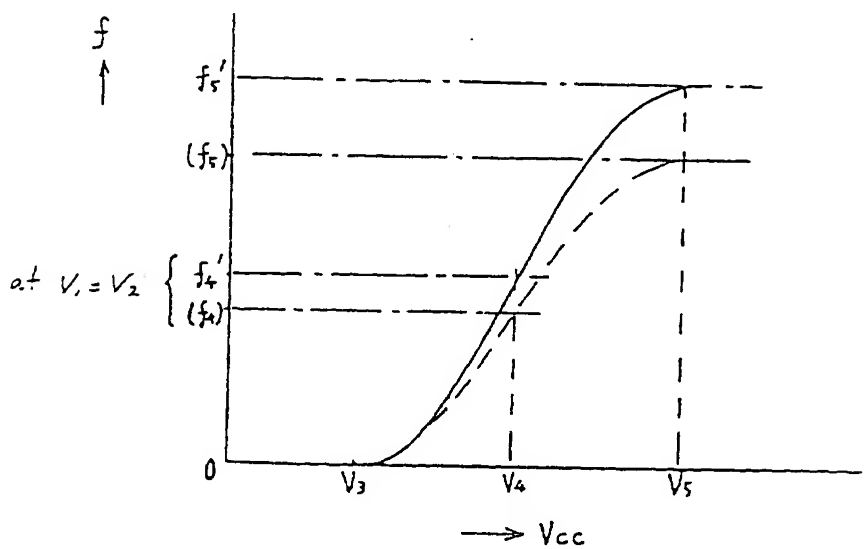
f
f_5'
(f_5)
at $V_1 = V_2$
f_4'
(f_4)
0
V_3
V_4
V_5
→ Vcc

FIG. 10

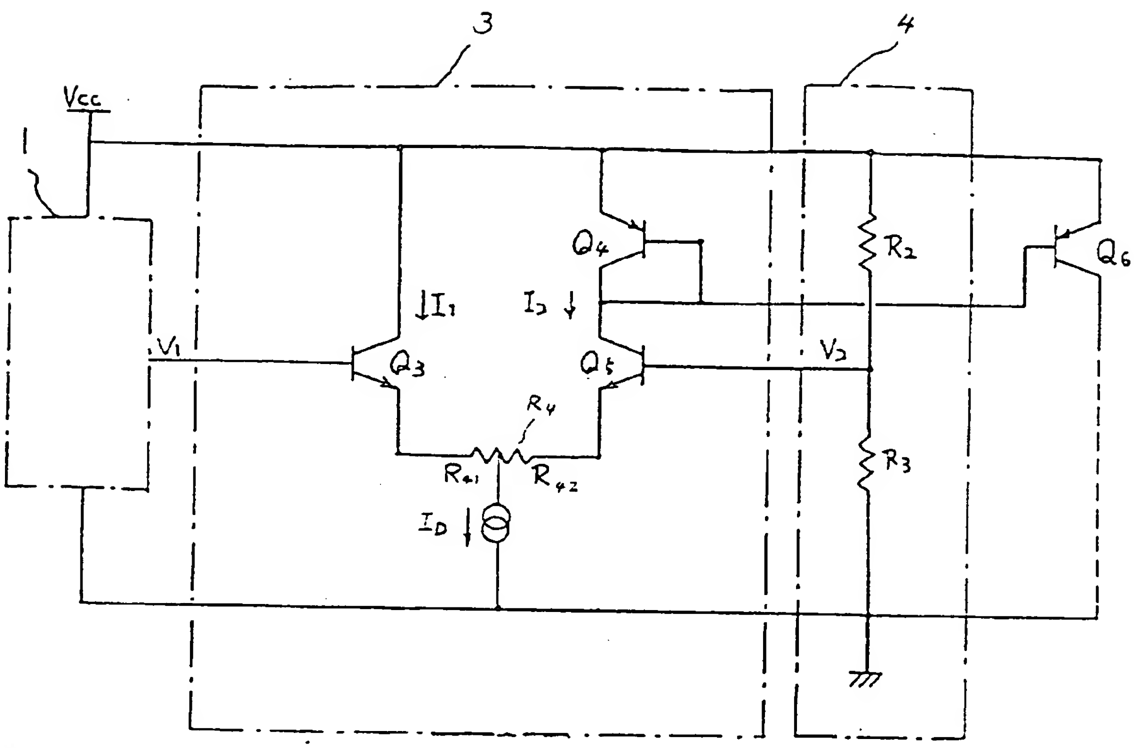

FIG.11

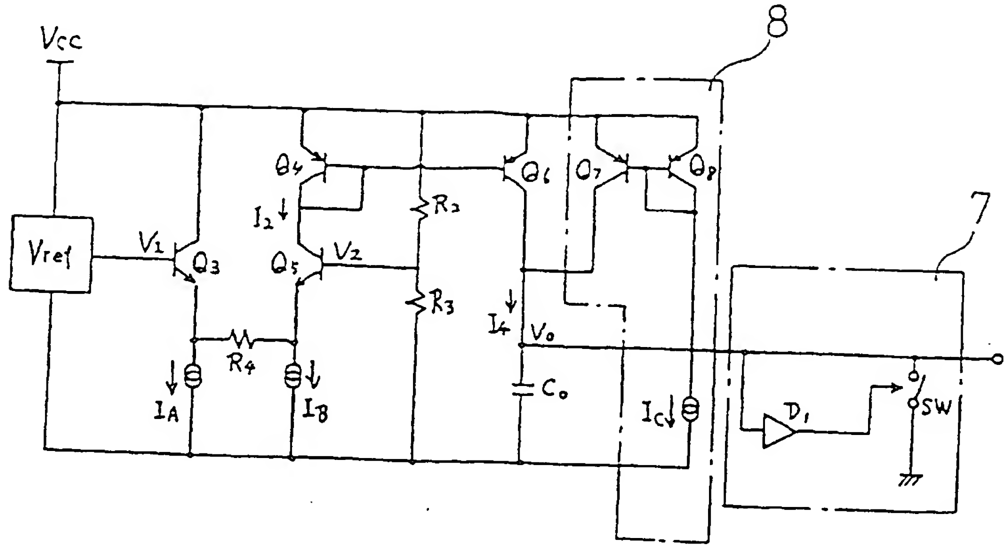
Vcc
8
Q4
Q6
Q7
Q8
R2
I2
7
Vref
V1
Q3
Q5
V2
R3
I4
V0
R4
IA
IB
C0
IC
D1
SW

FIG.12

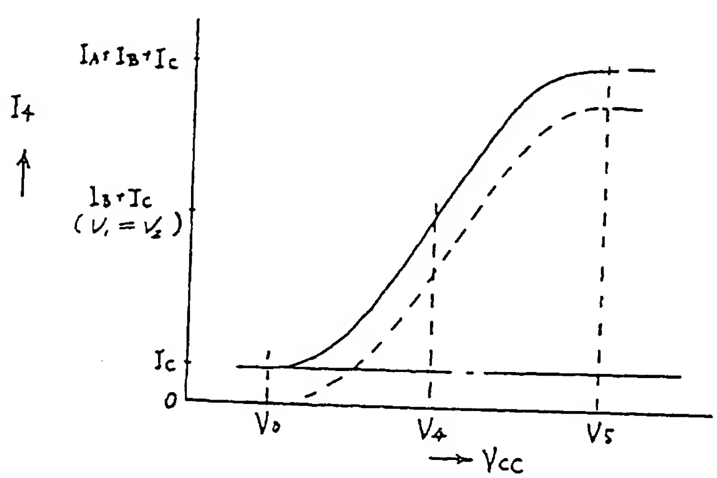
IA+IB+IC
I4
IB+IC
(V1 = V2)
IC
0
V0
V4
V5
Vcc

FIG. 13

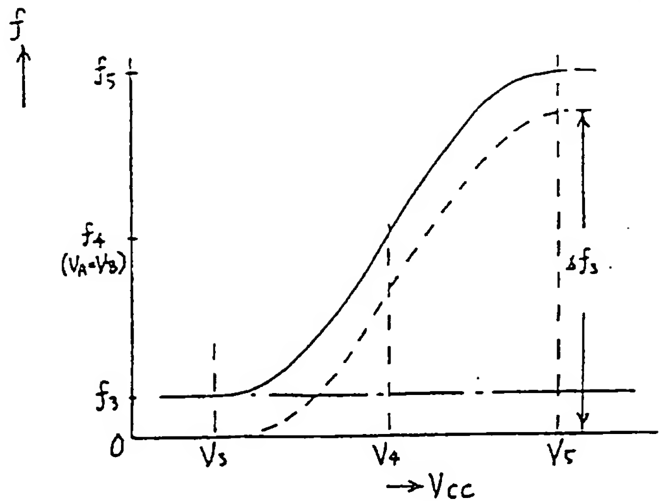
f
f5
f4
(VA=VB)
f3
0
V3
V4
V5
→Vcc
Δf3

FIG. 14

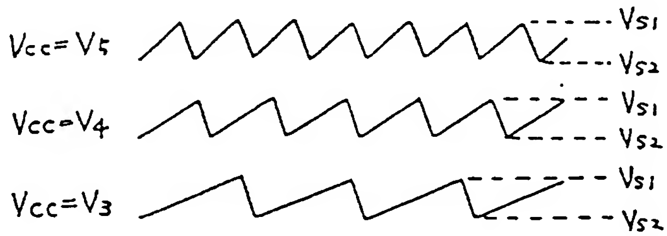
Vcc=V5
Vcc=V4
Vcc=V3
Vs1
Vs2
Vs1
Vs2
Vs1
Vs2

FIG. 15

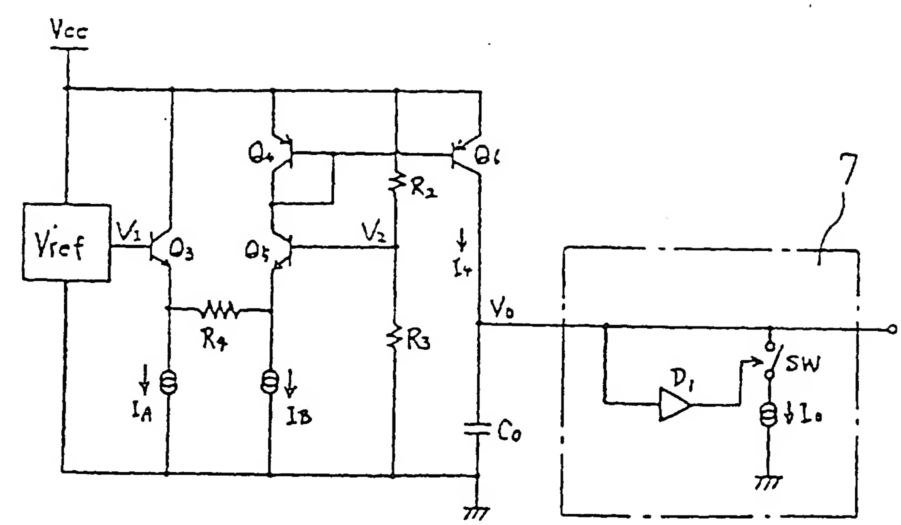

FIG. 16

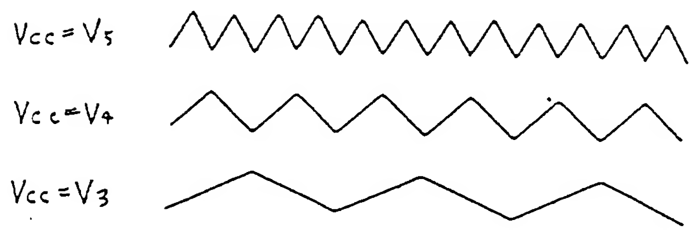
Vcc = V5
Vcc = V4
Vcc = V3

FIG. 17

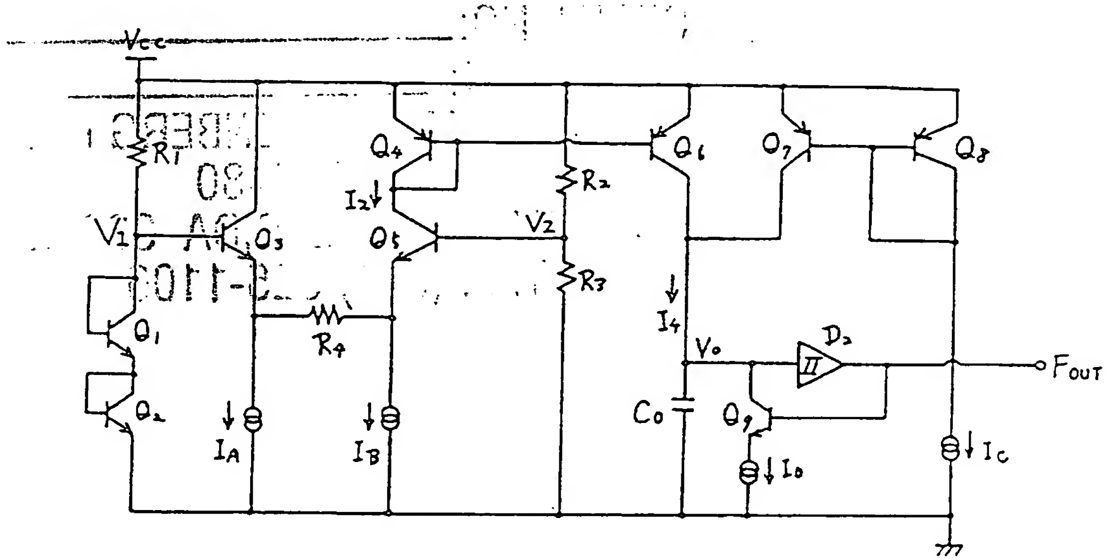
Vcc
R1
V1
Q3
Q1
Q2
IA
Q4
I2
Q5
R4
IB
V2
R2
R3
Q6
Q7
Q8
I4
V0
D2
C0
Q9
I0
Ic
FOUT

FIG. 18

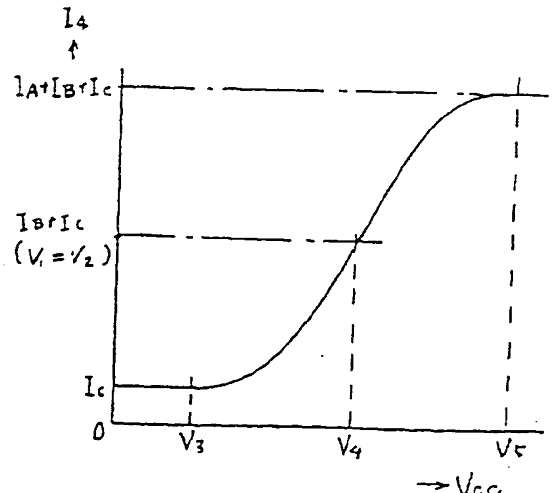

FIG. 19

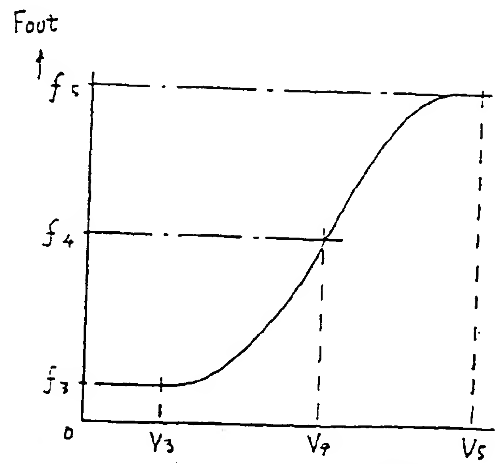

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FIG. 20